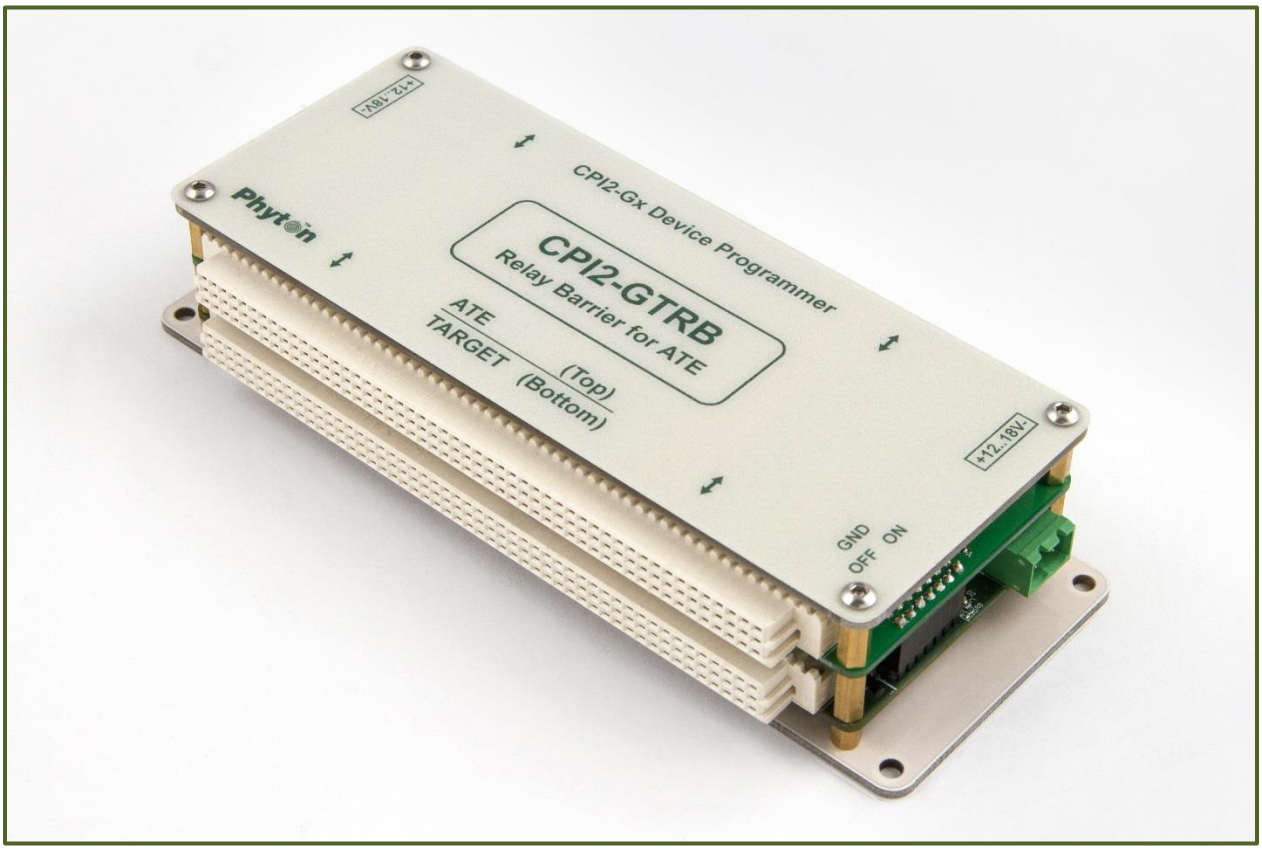
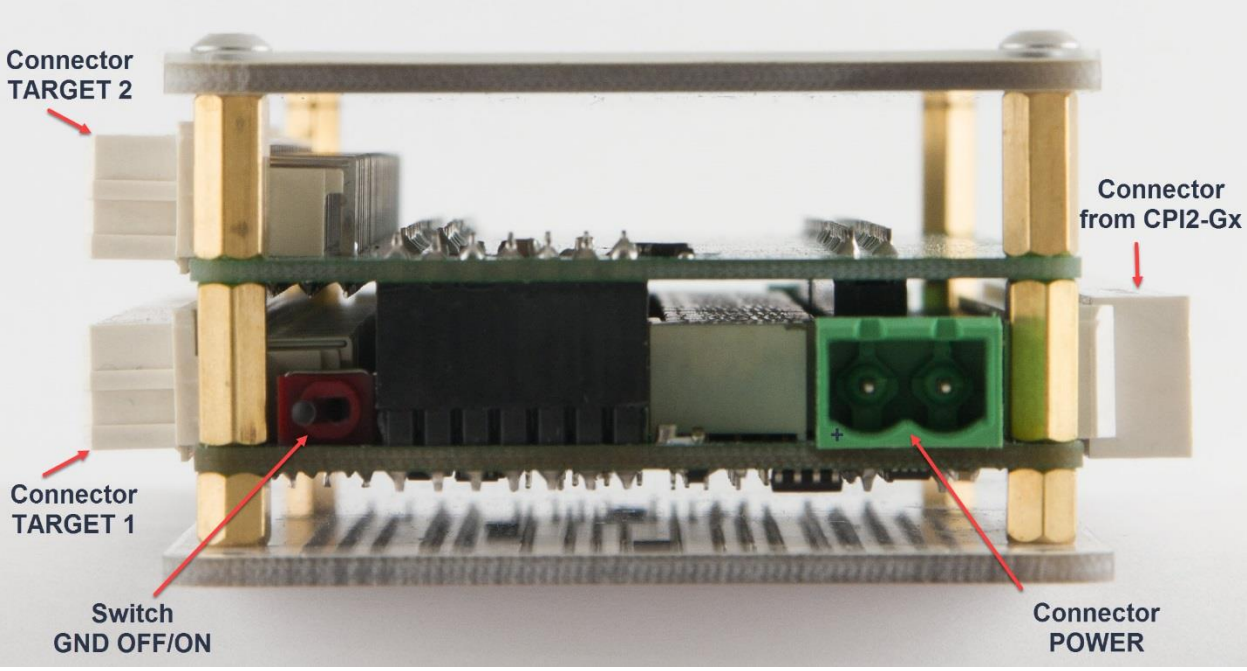
CPI2-GTRB Relay Barrier

CPI2-GTRB relay barrier, shown on the picture below, is intended for disconnecting CPI2-Gx gang device programmers from target boards presumably while they are under functional testing.

This relay barrier uses miniature electromechanical relays for switching logical ISP signal lines (7 sites by 12 ISP signals in each) and GND (ground) lines (7 sites by 9 GND signals in each).



A CPI2-GTRB unit should be powered from an external 12 to 18V@2A power supply. The unit has a couple of two-pin green power connectors to plug a cable or wires from the power adapter, which can be connected to either side, wherever it is more convenient. These connectors are located on both short end faces of the CPI2-GTRB unit. See the CPI2-GTRB side view below.

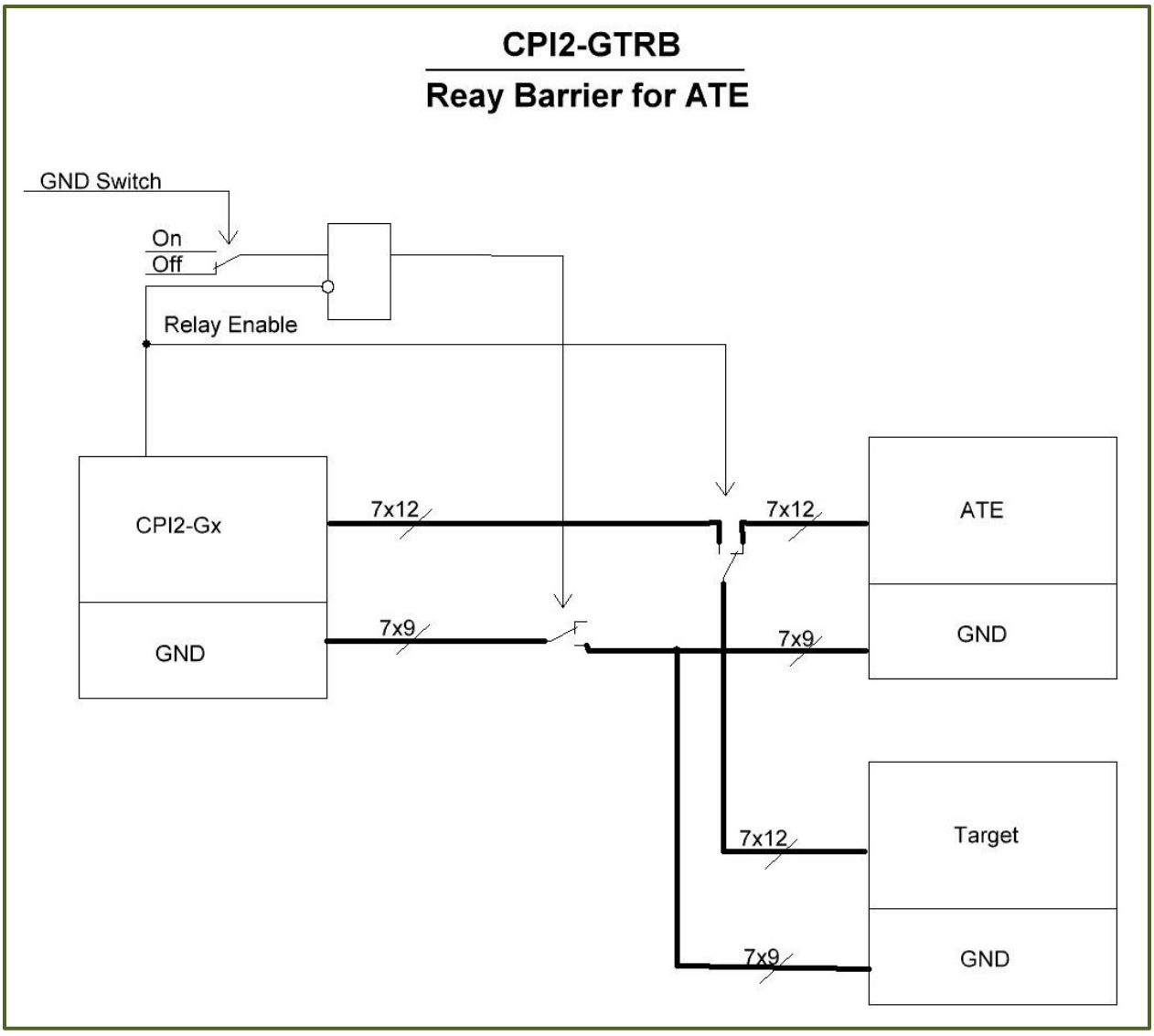


A CPI2-GTRB unit docks to female type **TARGET – channel A** or **TARGET – channel B** 150-pin DIN connectors installed on CPI2-Gx device programmers by a male type complimentary connector marked on the top label as **CPI2-Gx Device Programmer.** This connector locates on a long rear side of the CPI2-GTRB unit.

It is possible to dock a couple of relay barrier units to both **A** and **B** channel connectors.

On an opposite, front site a CPI2-GTRB unit has a pair of female type 150-pin DIN connectors. The bottom one, marked as **TARGET (Bottom)**, is intended for connecting ISP signals and ground lines to target PCB panels**.** The top connector can be *optionally* used for connecting to the test equipment; it is marked as **ATE (Top)**. In case when programming target PCB panels is combined with functional testing, use of these two connectors enables permanent keeping automated testers connected to a target panel, *excluding* those short periods of time while the CPI2-Gx programs, reads or maintains other operations on the DUTs installed on the target panel.

See the CPI2-GTRB flowchart below.



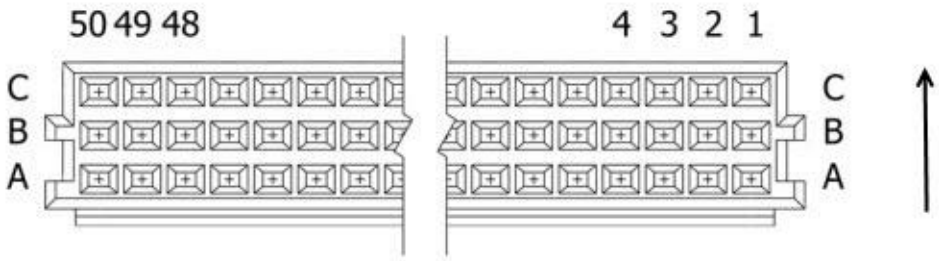
In the idle mode a CPI2-Gx gang device programmer keeps relays inside of the CPI2-GTRB unit inactive, so the ISP signals and ground lines coming from the CPI2-Gx device programmer remain disconnected from the target panel and ATE lines. In this mode the target panel remains connected to the ATE enabling functional testing. Only when the programmer operates on the target panel, i.e. it executes an **Auto Program** batch of command it issues the **Relay Enable** signal that switches relays on and connects ISP signals and ground lines to the target.

The barrier enables two modes for switching ground lines between the programmer and target:
- **GND ON** - when the ground lines on the CPI2-Gx TARGET connector remain always connected to the ground circuit of the target, even while the relays disconnect ISP signals from the target panel;
- **GND OFF** – when the CPI2-Gx ground lines are disconnected synchronously with the ISP signals and remains disconnected between executing **Auto Program** batch of command.

Switching between the **GND ON** and **GND OFF** modes is controlled manually by a miniature switch located on one side of the unit and marked on the top of the CPI2-GTRB unit as **GND/ ON-OFF**.

Connectors TARGET

150-pin DIN connectors installed on the CPI2-GTRB unit have the following pinout:



The matrix below shows pinouts of ISP and GND signals on the input male type connector located on a rear side of the relay barrier unit docking to the CPI2-Gx device programmer's **TARGET - channel A** and **TARGET - channel B** outputs.

← (male type input connector) **"to CPI2-Gx Device Programmer"**

Pin #	Pin Name	Description	Pin #	Pin Name	Description	Pin #	Pin Name	Description
A1	1/PA1	Site1: digital IO pin1	**B1**	GND	**Ground**	**C1**	1/PA7	Site1: digital IO pin7
A2	1/PA2	Site1: digital IO pin2	**B2**	GND	**Ground**	**C2**	1/PA8	Site1: digital IO pin8
A3	1/PA3	Site1: digital IO pin3	**B3**	GND	**Ground**	**C3**	1/PA9	Site1: digital IO pin9
A4	1/PA4	Site1: digital IO pin4	**B4**	GND	**Ground**	**C4**	1/PA10	Site1: digital IO pin10
A5	1/PA5	Site1: digital IO pin5	**B5**	GND	**Ground**	**C5**	1/PA11	Site1: digital IO pin11
A6	1/PA6	Site1: digital IO pin6	**B6**	GND	**Ground**	**C6**	1/PA12	Site1: digital IO pin12
A7	**DNU**	**Reserved for Phyton use***	**B7**	GND	**Ground**	**C7**	**DNU**	**Reserved for Phyton use***
A8	2/PA1	Site2: digital IO pin1	**B8**	GND	**Ground**	**C8**	2/PA7	Site2: digital IO pin7
A9	2/PA2	Site2: digital IO pin2	**B9**	GND	**Ground**	**C9**	2/PA8	Site2: digital IO pin8
A10	2/PA3	Site2: digital IO pin3	**B10**	GND	**Ground**	**C10**	2/PA9	Site2: digital IO pin9
A11	2/PA4	Site2: digital IO pin4	**B11**	GND	**Ground**	**C11**	2/PA10	Site2: digital IO pin10
A12	2/PA5	Site2: digital IO pin5	**B12**	GND	**Ground**	**C12**	2/PA11	Site2: digital IO pin11
A13	2/PA6	Site2: digital IO pin6	**B13**	GND	**Ground**	**C13**	2/PA12	Site2: digital IO pin12
A14	**DNU**	**Reserved for Phyton use***	**B14**	GND	**Ground**	**C14**	**DNU**	**Reserved for Phyton use***
A15	3/PA1	Site3: digital IO pin1	**B15**	GND	**Ground**	**C15**	3/PA7	Site3: digital IO pin7
A16	3/PA2	Site3: digital IO pin2	**B16**	GND	**Ground**	**C16**	3/PA8	Site3: digital IO pin8
A17	3/PA3	Site3: digital IO pin3	**B17**	GND	**Ground**	**C17**	3/PA9	Site3: digital IO pin9
A18	3/PA4	Site3: digital IO pin4	**B18**	GND	**Ground**	**C18**	3/PA10	Site3: digital IO pin10
A19	3/PA5	Site3: digital IO pin5	**B19**	GND	**Ground**	**C19**	3/PA11	Site3: digital IO pin11
A20	3/PA6	Site3: digital IO pin6	**B20**	GND	**Ground**	**C20**	3/PA12	Site3: digital IO pin12
A21	**DNU**	**Reserved for Phyton use***	**B21**	GND	**Ground**	**C21**	**DNU**	**Reserved for Phyton use***
A22	GND	**Ground**	**B22**	GND	**Ground**	**C22**	GND	**Ground**
A23	4/PA1	Site4: digital IO pin1	**B23**	GND	**Ground**	**C23**	4/PA7	Site4: digital IO pin7
A24	4/PA2	Site4: digital IO pin2	**B24**	GND	**Ground**	**C24**	4/PA8	Site4: digital IO pin8
A25	4/PA3	Site4: digital IO pin3	**B25**	GND	**Ground**	**C25**	4/PA9	Site4: digital IO pin9
A26	4/PA4	Site4: digital IO pin4	**B26**	GND	**Ground**	**C26**	4/PA10	Site4: digital IO pin10

A27	4/PA5	Site4: digital IO pin5	**B27**	GND	**Ground**	**C27**	4/PA11	Site4: digital IO pin11
A28	4/PA6	Site4: digital IO pin6	**B28**	GND	**Ground**	**C28**	4/PA12	Site4: digital IO pin12
A29	**DNU**	**Reserved for Phyton use***	**B29**	GND	**Ground**	**C29**	**DNU**	**Reserved for Phyton use***
A30	**DNU**	**Reserved for Phyton use***	**B30**	GND	**Ground**	**C30**	**DNU**	**Reserved for Phyton use***
A31	5/PA1	Site5: digital IO pin1	**B31**	GND	**Ground**	**C31**	5/PA7	Site5: digital IO pin7
A32	5/PA2	Site5: digital IO pin2	**B32**	GND	**Ground**	**C32**	5/PA8	Site5: digital IO pin8
A33	5/PA3	Site5: digital IO pin3	**B33**	GND	**Ground**	**C33**	5/PA9	Site5: digital IO pin9
A34	5/PA4	Site5: digital IO pin4	**B34**	GND	**Ground**	**C34**	5/PA10	Site5: digital IO pin10
A35	5/PA5	Site5: digital IO pin5	**B35**	GND	**Ground**	**C35**	5/PA11	Site5: digital IO pin11
A36	5/PA6	Site5: digital IO pin6	**B36**	GND	**Ground**	**C36**	5/PA12	Site5: digital IO pin12
A37	**DNU**	**Reserved for Phyton use***	**B37**	GND	**Ground**	**C37**	**DNU**	**Reserved for Phyton use***
A38	6/PA1	Site6: digital IO pin1	**B38**	GND	**Ground**	**C38**	6/PA7	Site6: digital IO pin7
A39	6/PA2	Site6: digital IO pin2	**B39**	GND	**Ground**	**C39**	6/PA8	Site6: digital IO pin8
A40	6/PA3	Site6: digital IO pin3	**B40**	GND	**Ground**	**C40**	6/PA9	Site6: digital IO pin9
A41	6/PA4	Site6: digital IO pin4	**B41**	GND	**Ground**	**C41**	6/PA10	Site6: digital IO pin10
A42	6/PA5	Site6: digital IO pin5	**B42**	GND	**Ground**	**C42**	6/PA11	Site6: digital IO pin11
A43	6/PA6	Site6: digital IO pin6	**B43**	GND	**Ground**	**C43**	6/PA12	Site6: digital IO pin12
A44	**DNU**	**Reserved for Phyton use***	**B44**	GND	**Ground**	**C44**	**DNU**	**Reserved for Phyton use***
A45	7/PA1	Site7: digital IO pin1	**B45**	GND	**Ground**	**C45**	7/PA7	Site7: digital IO pin7
A46	7/PA2	Site7: digital IO pin2	**B46**	GND	**Ground**	**C46**	7/PA8	Site7: digital IO pin8
A47	7/PA3	Site7: digital IO pin3	**B47**	GND	**Ground**	**C47**	7/PA9	Site7: digital IO pin9
A48	7/PA4	Site7: digital IO pin4	**B48**	GND	**Ground**	**C48**	7/PA10	Site7: digital IO pin10
A49	7/PA5	Site7: digital IO pin5	**B49**	GND	**Ground**	**C49**	7/PA11	Site7: digital IO pin11
A50	7/PA6	Site7: digital IO pin6	**B50**	GND	**Ground**	**C50**	7/PA12	Site7: digital IO pin12

The matrix below shows ISP and GND signal pinouts of **TARGET (Bottom)** and **ATE (Top)** “output” connectors located on a front side of the CPI2-GTRB relay barrier unit. Both these connectors have identical pinouts.

--< (female type output connectors) **Target (Bottom)** and **ATE (Top)**

Pin #	Pin Name	Description	Pin #	Pin Name	Description	Pin #	Pin Name	Description
A1	1/PA1	Site1: digital IO pin1	**B1**	1/GND	**Site#1 Ground**	**C1**	1/PA7	Site1: digital IO pin7
A2	1/PA2	Site1: digital IO pin2	**B2**	1/GND	**Site#1 Ground**	**C2**	1/PA8	Site1: digital IO pin8
A3	1/PA3	Site1: digital IO pin3	**B3**	1/GND	**Site#1 Ground**	**C3**	1/PA9	Site1: digital IO pin9
A4	1/PA4	Site1: digital IO pin4	**B4**	1/GND	**Site#1 Ground**	**C4**	1/PA10	Site1: digital IO pin10
A5	1/PA5	Site1: digital IO pin5	**B5**	1/GND	**Site#1 Ground**	**C5**	1/PA11	Site1: digital IO pin11
A6	1/PA6	Site1: digital IO pin6	**B6**	1/GND	**Site#1 Ground**	**C6**	1/PA12	Site1: digital IO pin12
A7	**DNU**	**Reserved for Phyton use***	**B7**	1/GND	**Site#1 Ground**	**C7**	**DNU**	**Reserved for Phyton use***
A8	2/PA1	Site2: digital IO pin1	**B8**	2/GND	**Site#2 Ground**	**C8**	2/PA7	Site2: digital IO pin7
A9	2/PA2	Site2: digital IO pin2	**B9**	2/GND	**Site#2 Ground**	**C9**	2/PA8	Site2: digital IO pin8
A10	2/PA3	Site2: digital IO pin3	**B10**	2/GND	**Site#2 Ground**	**C10**	2/PA9	Site2: digital IO pin9
A11	2/PA4	Site2: digital IO pin4	**B11**	2/GND	**Site#2 Ground**	**C11**	2/PA10	Site2: digital IO pin10
A12	2/PA5	Site2: digital IO pin5	**B12**	2/GND	**Site#2 Ground**	**C12**	2/PA11	Site2: digital IO pin11
A13	2/PA6	Site2: digital IO pin6	**B13**	2/GND	**Site#2 Ground**	**C13**	2/PA12	Site2: digital IO pin12

A14	**DNU**	**Reserved for Phyton use***	**B14**	2/GND	**Site#2 Ground**	**C14**	**DNU**	**Reserved for Phyton use***
A15	3/PA1	Site3: digital IO pin1	**B15**	3/GND	**Site#3 Ground**	**C15**	3/PA7	Site3: digital IO pin7
A16	3/PA2	Site3: digital IO pin2	**B16**	3/GND	**Site#3 Ground**	**C16**	3/PA8	Site3: digital IO pin8
A17	3/PA3	Site3: digital IO pin3	**B17**	3/GND	**Site#3 Ground**	**C17**	3/PA9	Site3: digital IO pin9
A18	3/PA4	Site3: digital IO pin4	**B18**	3/GND	**Site#3 Ground**	**C18**	3/PA10	Site3: digital IO pin10
A19	3/PA5	Site3: digital IO pin5	**B19**	3/GND	**Site#3 Ground**	**C19**	3/PA11	Site3: digital IO pin11
A20	3/PA6	Site3: digital IO pin6	**B20**	3/GND	**Site#3 Ground**	**C20**	3/PA12	Site3: digital IO pin12
A21	**DNU**	**Reserved for Phyton use***	**B21**	3/GND	**Site#3 Ground**	**C21**	**DNU**	**Reserved for Phyton use***
A22	3/GND	**Site#3 Ground**	**B22**	3/GND	**Site#3 Ground**	**C22**	3/GND	**Site#3 Ground**
A23	4/PA1	Site4: digital IO pin1	**B23**	4/GND	**Site#4 Ground**	**C23**	4/PA7	Site4: digital IO pin7
A24	4/PA2	Site4: digital IO pin2	**B24**	4/GND	**Site#4 Ground**	**C24**	4/PA8	Site4: digital IO pin8
A25	4/PA3	Site4: digital IO pin3	**B25**	4/GND	**Site#4 Ground**	**C25**	4/PA9	Site4: digital IO pin9
A26	4/PA4	Site4: digital IO pin4	**B26**	4/GND	**Site#4 Ground**	**C26**	4/PA10	Site4: digital IO pin10
A27	4/PA5	Site4: digital IO pin5	**B27**	4/GND	**Site#4 Ground**	**C27**	4/PA11	Site4: digital IO pin11
A28	4/PA6	Site4: digital IO pin6	**B28**	4/GND	**Site#4 Ground**	**C28**	4/PA12	Site4: digital IO pin12
A29	**DNU**	**Reserved for Phyton use***	**B29**	4/GND	**Site#4 Ground**	**C29**	**DNU**	**Reserved for Phyton use***
A30	**DNU**	**Reserved for Phyton use***	**B30**	5/GND	**Site#5 Ground**	**C30**	**DNU**	**Reserved for Phyton use***
A31	5/PA1	Site5: digital IO pin1	**B31**	5/GND	**Site#5 Ground**	**C31**	5/PA7	Site5: digital IO pin7
A32	5/PA2	Site5: digital IO pin2	**B32**	5/GND	**Site#5 Ground**	**C32**	5/PA8	Site5: digital IO pin8
A33	5/PA3	Site5: digital IO pin3	**B33**	5/GND	**Site#5 Ground**	**C33**	5/PA9	Site5: digital IO pin9
A34	5/PA4	Site5: digital IO pin4	**B34**	5/GND	**Site#5 Ground**	**C34**	5/PA10	Site5: digital IO pin10
A35	5/PA5	Site5: digital IO pin5	**B35**	5/GND	**Site#5 Ground**	**C35**	5/PA11	Site5: digital IO pin11
A36	5/PA6	Site5: digital IO pin6	**B36**	5/GND	**Site#5 Ground**	**C36**	5/PA12	Site5: digital IO pin12
A37	**DNU**	**Reserved for Phyton use***	**B37**	6/GND	**Site#6 Ground**	**C37**	**DNU**	**Reserved for Phyton use***
A38	6/PA1	Site6: digital IO pin1	**B38**	6/GND	**Site#6 Ground**	**C38**	6/PA7	Site6: digital IO pin7
A39	6/PA2	Site6: digital IO pin2	**B39**	6/GND	**Site#6 Ground**	**C39**	6/PA8	Site6: digital IO pin8
A40	6/PA3	Site6: digital IO pin3	**B40**	6/GND	**Site#6 Ground**	**C40**	6/PA9	Site6: digital IO pin9
A41	6/PA4	Site6: digital IO pin4	**B41**	6/GND	**Site#6 Ground**	**C41**	6/PA10	Site6: digital IO pin10
A42	6/PA5	Site6: digital IO pin5	**B42**	6/GND	**Site#6 Ground**	**C42**	6/PA11	Site6: digital IO pin11
A43	6/PA6	Site6: digital IO pin6	**B43**	6/GND	**Site#6 Ground**	**C43**	6/PA12	Site6: digital IO pin12
A44	**DNU**	**Reserved for Phyton use***	**B44**	7/GND	**Site#7 Ground**	**C44**	**DNU**	**Reserved for Phyton use***
A45	7/PA1	Site7: digital IO pin1	**B45**	7/GND	**Site#7 Ground**	**C45**	7/PA7	Site7: digital IO pin7
A46	7/PA2	Site7: digital IO pin2	**B46**	7/GND	**Site#7 Ground**	**C46**	7/PA8	Site7: digital IO pin8
A47	7/PA3	Site7: digital IO pin3	**B47**	7/GND	**Site#7 Ground**	**C47**	7/PA9	Site7: digital IO pin9
A48	7/PA4	Site7: digital IO pin4	**B48**	7/GND	**Site#7 Ground**	**C48**	7/PA10	Site7: digital IO pin10
A49	7/PA5	Site7: digital IO pin5	**B49**	7/GND	**Site#7 Ground**	**C49**	7/PA11	Site7: digital IO pin11
A50	7/PA6	Site7: digital IO pin6	**B50**	7/GND	**Site#7 Ground**	**C50**	7/PA12	Site7: digital IO pin12

Where:

- Signals marked as **DNU - Reserved for Phyton use***, may not be used by CPI2-GTRB barrier users. These connector pins should be left untouched.

- Site#/PAn and Site#/PBn (n=1...10) - logical signals formed by the CPI2-Gx high-speed buffers that can output target-specific logic 0 or 1, Vcc or GND levels, according to the chosen target

device type. The buffers are bidirectional, also serving as inputs when the programmer reads data.

- Site#/PAm and Site#/PBm (m=11 & 12) – signals formed by CPI2-Gx high speed mixed-signal circuits that can also output target-specific logic 0 or 1, Vpp or GND levels according to the type of the chosen target device. These lines can output Vcc with levels from 1.2 to 5.5V @ up to 350mA. The mixed-signal buffers are bidirectional, also serving as inputs when the <%CPN%> programmer reads data. In addition, these two signals can output Vpp voltage with levels from 1.5V to 15V @ up to 100mA.